REMARKS

The Office Action dated June 3, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

By this Amendment, claims 3 and 6 have been cancelled and claims 1, 5, 7 and 9 have been amended. Applicants submit that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1, 5, 7 and 9-12 are pending in the present application and are respectfully submitted for consideration.

Claims 1, 5, 7, 9 and 10 Recite Patentable Subject Matter

Claims 1, 3, 5-7, 9 and 10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Imura et al. (U.S. Patent No. 5,398,212, hereinafter "Imura"). Claims 3 and 6 have been cancelled, rendering these claims moot with regard to this rejection, and claims 1, 5, 7 and 9 have been amended. Applicants submit that each of claims 1, 5, 7, 9 and 10 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 1 recites a semiconductor memory device comprising a plurality of memory cells corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, where n is a positive integer; an invalid address detecting circuit detecting that an address signal supplied from exterior indicates an address space other than the address space; an invalid signal outputting circuit outputting an invalid signal via a dedicated terminal to the exterior of the semiconductor memory device when the invalid address detecting circuit carries out the detection; a latch circuit latching read data read from the memory cells in

each read operation; and an output controlling circuit outputting, without accessing the memory cells, the read data latched in the latch circuit by the preceding read operation, when the invalid address detecting circuit carries out the detection in a read operation.

Claim 5 recites a semiconductor memory device comprising a plurality of memory cells corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, where n is a positive integer; an invalid address detecting circuit detecting that an address signal supplied from exterior indicates an address space other than the address space; a latch circuit latching read data read from the memory cells in each read operation; and an output controlling circuit outputting, without accessing the memory cells, the read data latched in the latch circuit by the preceding read operation, when the invalid address detecting circuit carries out the detection in a read operation.

Claim 9 recites a method of controlling a semiconductor memory device comprising a plurality of memory cells corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, where n is a positive integer, the method comprising the steps of latching read data read from the memory cells in each read operation; and outputting an invalid signal via a dedicated terminal to the exterior of the semiconductor memory device, and outputting, without accessing the memory cells, the read data latched by the preceding read operation, when an address signal supplied from the exterior indicating an address space other than the address space has been detected.

The Office Action characterized Imura as showing a memory cell array 3 with address signal A_0- A_n, an empty address detecting circuit 5, an output buffer circuit 4 for outputting high impedance state thereby indicating that the address signal is invalid, DATA D_0- D_i, and control circuit 6. The Office Action also highlighted Table 2, column 8,

lines 21-67 along with Figure 2, column 6, lines 52-54 of Imura for allegedly showing the features recited in claims 1, 5 and 9.

Applicants respectfully submit that Imura fails to teach or suggest at least "a latch circuit latching read data read from the memory cells in each read operation; and an output controlling circuit outputting, without accessing the memory cells, the read data latched in the latch circuit by the preceding read operation, when the invalid address detecting circuit carries out the detection in a read operation."

In one exemplary embodiment of the present invention, a latch circuit is controlled by an output controlling circuit, and the latch circuit is for latching data read from the memory cells each time a read operation is performed. In addition, the output controlling circuit outputs the read data which is latched in the latch circuit by performing the preceding read operation when an invalid address is detected. The output controlling circuit outputs the read data without accessing the memory cells.

To qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Imura fails to disclose or suggest each and every feature of claim 1. Accordingly, Applicants respectfully submit that claim 1 is not anticipated by nor rendered obvious by the disclosure of Imura. Therefore, Applicants respectfully submit that claim 1 is allowable.

Claim 7 is dependent on claim 1 and claim 10 is dependent on claim 9. As such, each of claims 7 and 10 is allowable due to its dependency on allowable claims 1 and 9, as well as the additional subject matter recited therein.

Accordingly, Applicants request withdrawal of the rejection.

Claims 11 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Imura. In making this rejection, the Examiner noted that Imura fails to "teach the deactivations of the decoder and the sense amplifer when the invalid address detecting circuit carries out the detection. The Examiner further took Official Notice that it would have been obvious to one skilled in the art at the time the invention was made to implement the semiconductor memory device as taught by Imura to include the deactivations of the address decoder and the sense amplifier.

Applicants agree that Imura fails to teach the deactivations of the decoder and the sense amplifier when the invalid address detecting circuit carries out the detection, yet respectfully traverse the Official Notice taken. It is submitted that it would not have been obvious to one skilled in the art at the time the invention was made to implement the semiconductor memory device as taught by Imura to include the deactivations of the address decoder and the sense amplifier as recited in the claims of the present application. Hence, Applicants submit that claims 11 and 12 are allowable.

In addition, as claims 11 and 12 depend from claim 1, Applicants submit that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claim.

Accordingly, Applicants request withdrawal of the rejection.

Conclusion

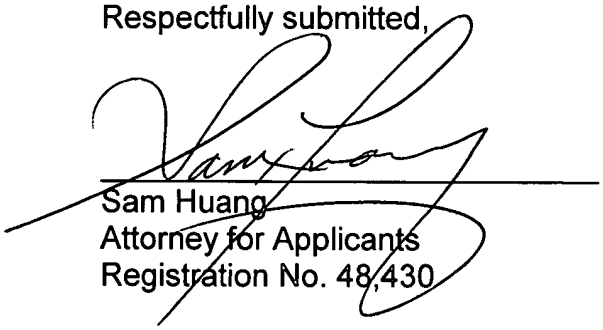
In view of the above, Applicants respectfully submit that each of claims 1, 5, 7 and 9-12 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that this subject matter is more than sufficient to render the claims

non-obvious to a person of ordinary skill in the art, and therefore, respectfully request that claims 1, 5, 7 and 9-12 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108397-00011.**

Respectfully submitted,



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